Zhouheng Sun
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Experience

- **SoC/ASIC Design Verification Engineer, Apple Inc.** Seattle, WA | Apr 2025 - Present
  - Lead the UVM-based verification (team of 3) of an SoC power management IP; coordinated verification deliverables and dependencies across 5+ full-chip, subsystem and subcomponent DV teams.
  - Create and review comprehensive test plans for the ASIC HW accelerator, including standalone HW verification based on FW contract and co-simulation with FW running on an embedded CPU.
  - Lead research and development of generative AI harnesses and workflows across a 50+ person organization targeting autonomous debugging and CI-based inconsistency detection.
  - Build formal verification setups for signal connectivity and liveness properties of core FSM logic using compositional reasoning.
- **CPU Formal Verification Engineer, Apple Inc.** Cupertino, CA | July 2021 - Apr 2025
  - Created formal verification environments to verify CPU memory system IP for M-series processors (performance core), focusing on security against speculative attacks and memory ordering correctness. Independently led verification of major components and features in the IP.
  - Found 50+ design bugs that were difficult to reproduce in post-silicon and conventional DV flows.
  - Formally verified and signed off on fixes for 10+ critical bugs during the ECO stage.
  - Applied formal techniques such as initial state abstraction to reduce solver complexity and increase bounded checking depth.
  - Built tooling for template-based property generation, live recompilation, and property queries.
- **Software Engineering Intern, Citadel Securities** Summer 2020
  - Verified an FPGA-accelerated pipeline against the software gold model, applied C++ template meta-programming for configurable FPGA interfaces, and optimized build scripts to reduce binary size by 80%.

Education

- **Stanford University** Stanford, CA
  M.S. Computer Science, Specialization: Software Theory. *Sept 2019 - June 2021*
- **The University of California, Los Angeles** Los Angeles, CA
  B.S. Computer Science, Minor in Mathematics, Magna Cum Laude. *Sept 2015 - June 2019*

Research & Projects

- **Student Researcher - Formal Hardware Verification at Stanford** Fall 2020 - Spring 2021
  - Used SAT/SMT solver to verify a custom AXI-to-CGRA interface IP for Stanford's AHA hardware project.
- **Student Researcher - Programming Language Lab at UCLA** Fall 2017 - Sep 2019
  - Led a prototyping effort to add first-order logic to a program-invariant synthesis engine in OCaml.
- **Personal Project: Puzzle solvers** Winter 2018 - Present
  - Created and maintained onionhoney's Roux Trainers, the most popular Roux method speed-cubing training app with ˜500 monthly active users.

Activities

- **Stanford CS 243 (Program Analysis and Optimization) Course Assistant** Jan 2021 - Mar 2021
- **ICPC (Competitive Programming) Club at UCLA ACM - Coach & President** Sep 2016 - Jun 2019

Contests and Awards

- **Competitive Programming**
  - 2019-20 ICPC North American Championship finalist; qualified for the ICPC World Finals; did not attend due to COVID-19.
  - Placed 5th out of 150 teams at 2019 ACM-ICPC Pacific Northwest Regional.
  - Placed 2nd out of 98 teams at 2018 ACM-ICPC Southern California Regional.
- **Speedcubing**
  - Achieved top-10 world rankings in multiple events.
  - Two-time Asian record holder, eleven-time China national record holder in WCA official events including 2x2 Cube, Rubik's Cube, One-handed solving, and 4x4 Cube.
  - 3rd place in USA National Rubik's Cube Championship 2023 One-Handed Event.
  - 9th place at Rubik's WCA World Championship 2025 One-Handed Event.

Skill Set

- Languages : Python, C, Verilog, SystemVerilog, Tcl, JavaScript, C++, Rust, OCaml.